



Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

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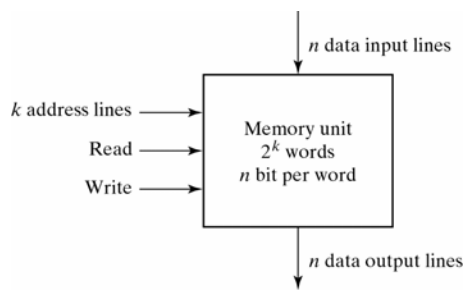


Fig. 7-2 Block Diagram of a Memory Unit

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Memory address		Memory content
Binary	decimal	
000000000	0	1011010101011101
000000001	1	1010101110001001
000000010	2	0000110101000110
	⋮	⋮
	⋮	⋮
111111101	1021	1001110100010100
111111110	1022	0000110100011110
111111111	1023	110111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

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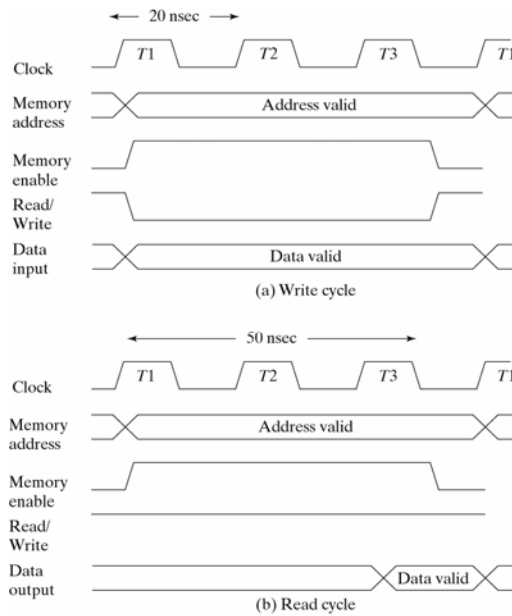
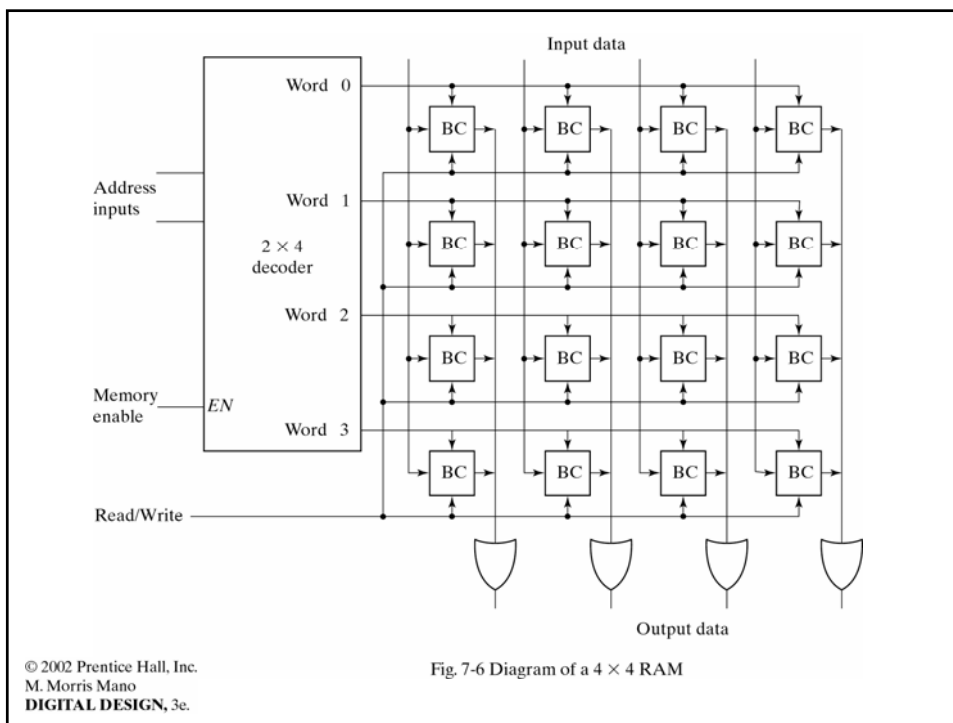
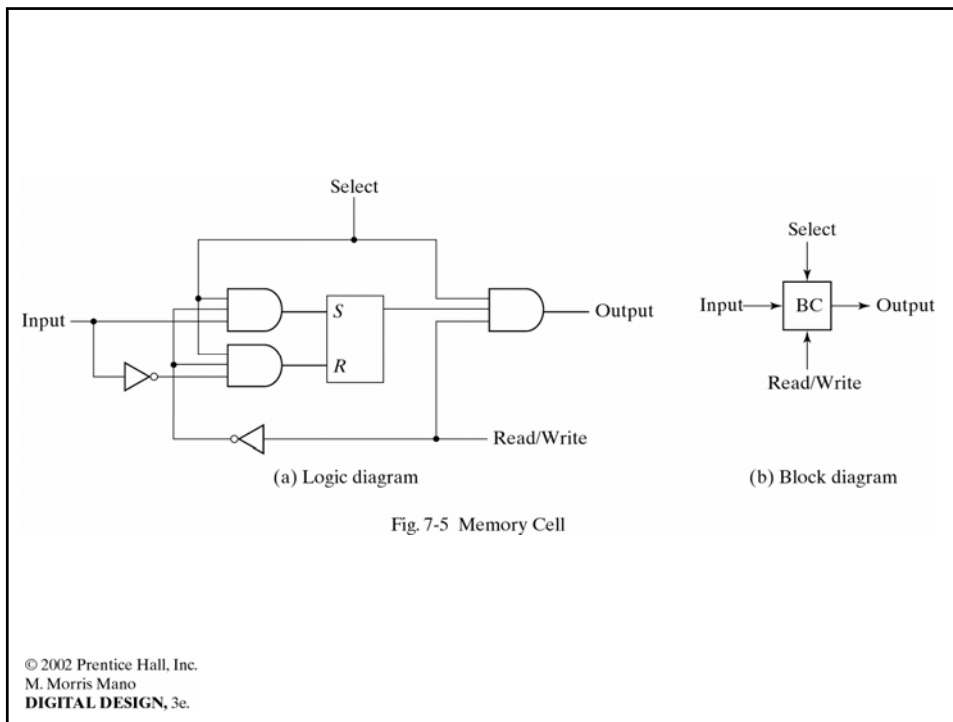
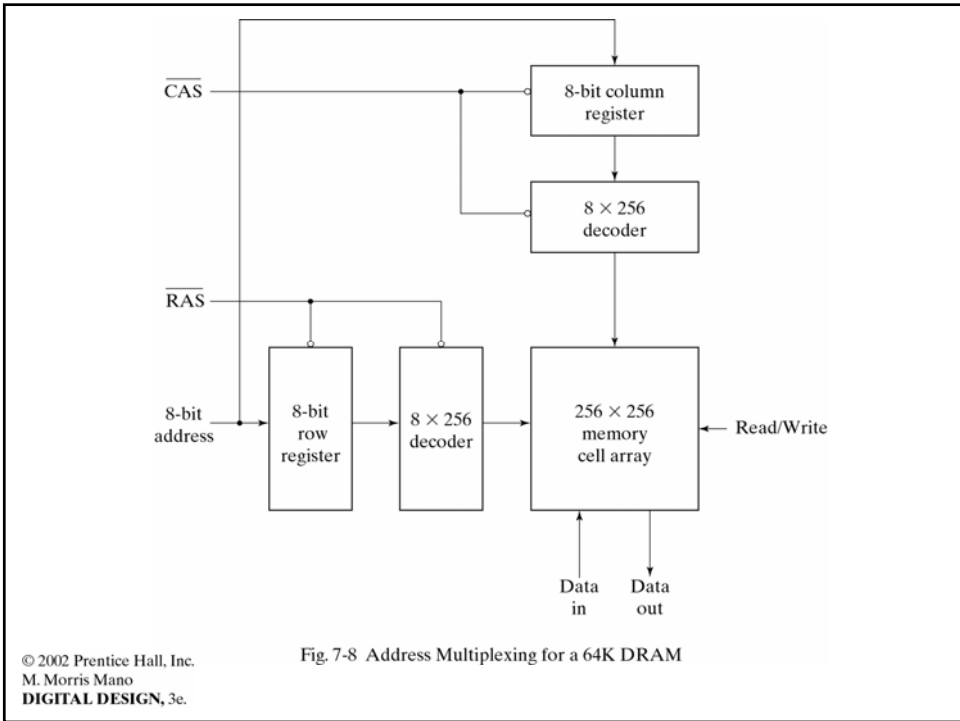
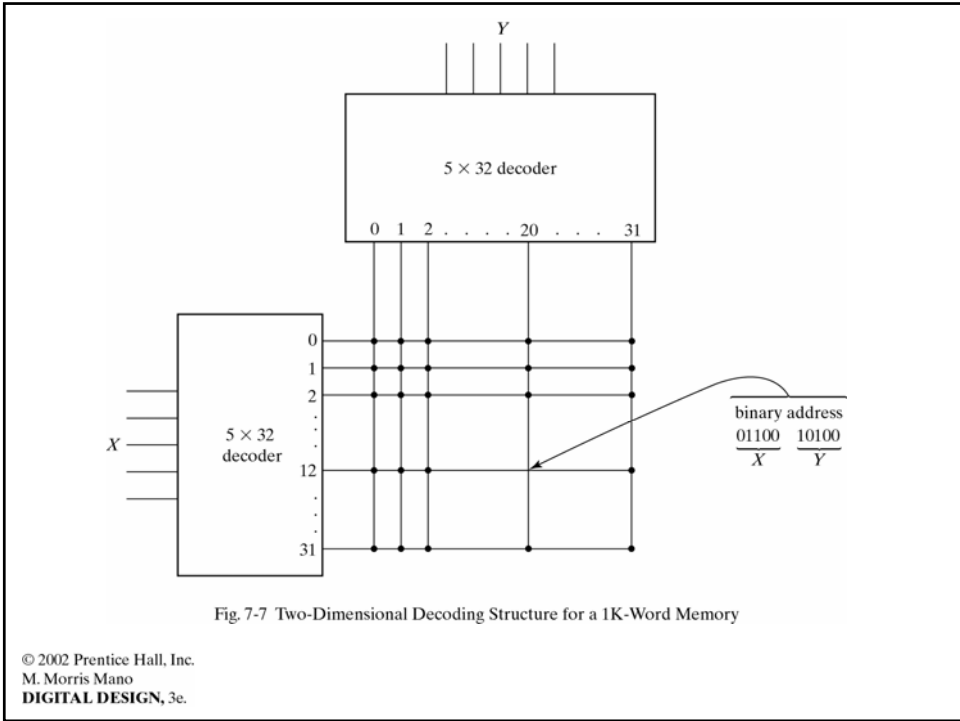


Fig. 7-4 Memory Cycle Timing Waveforms

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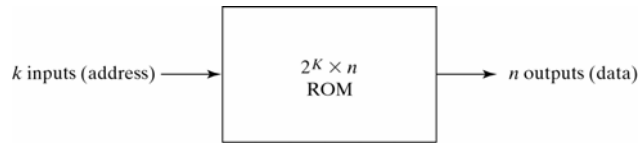


Fig. 7-9 ROM Block Diagram

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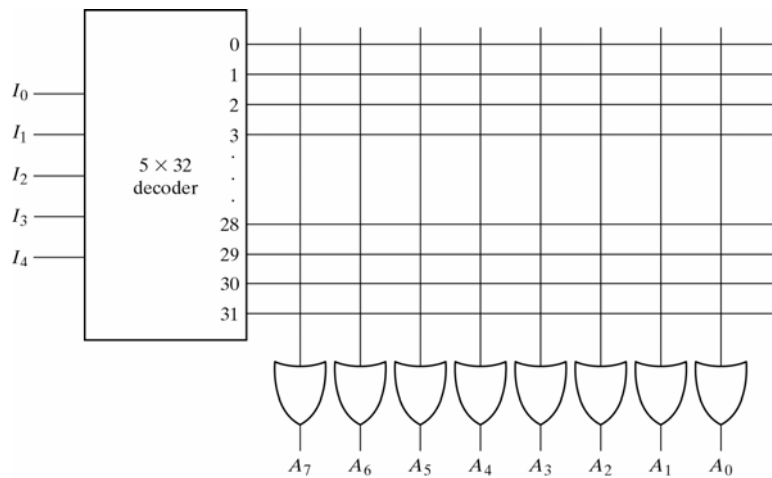
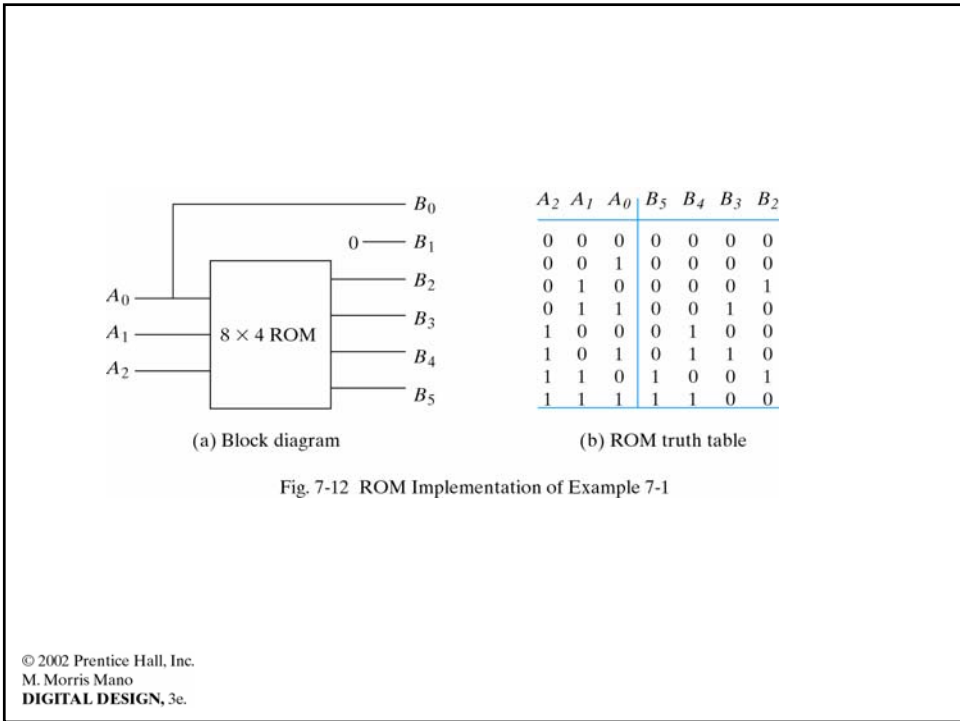
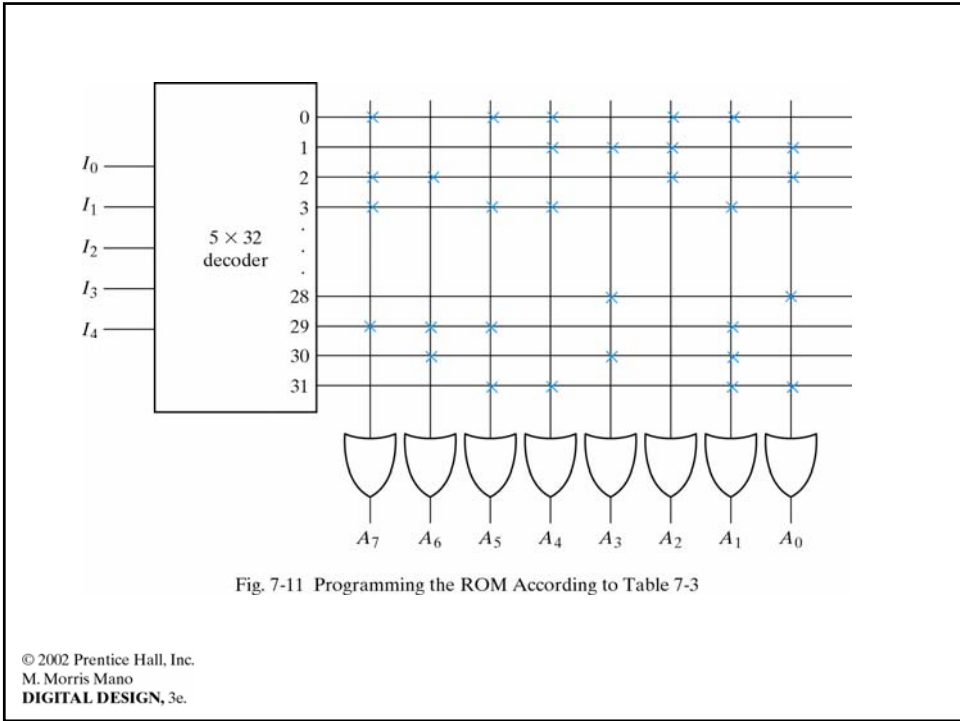
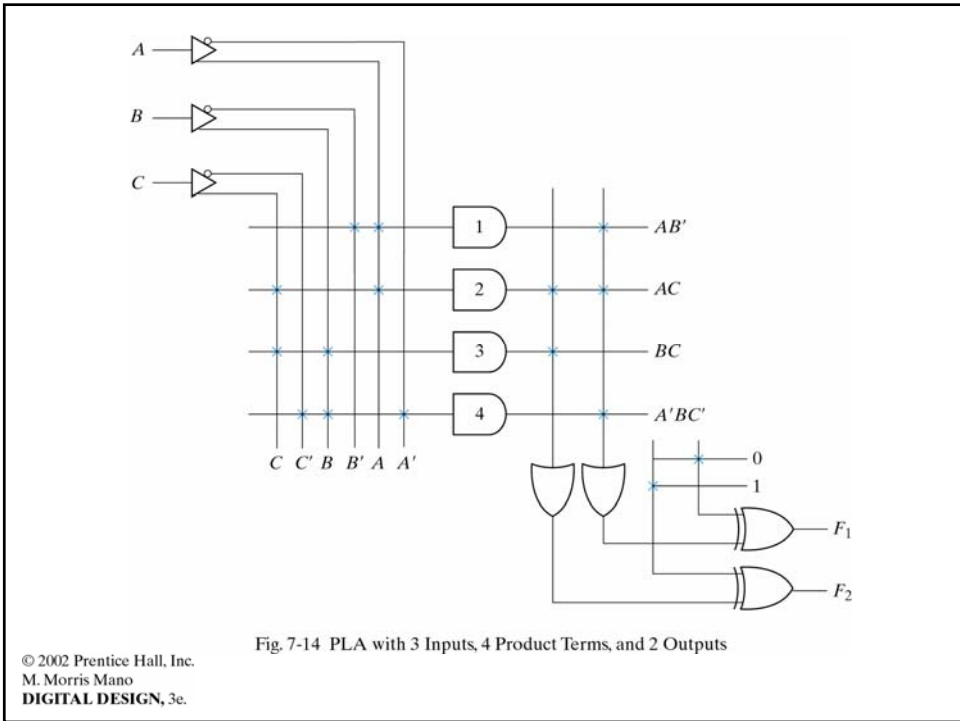
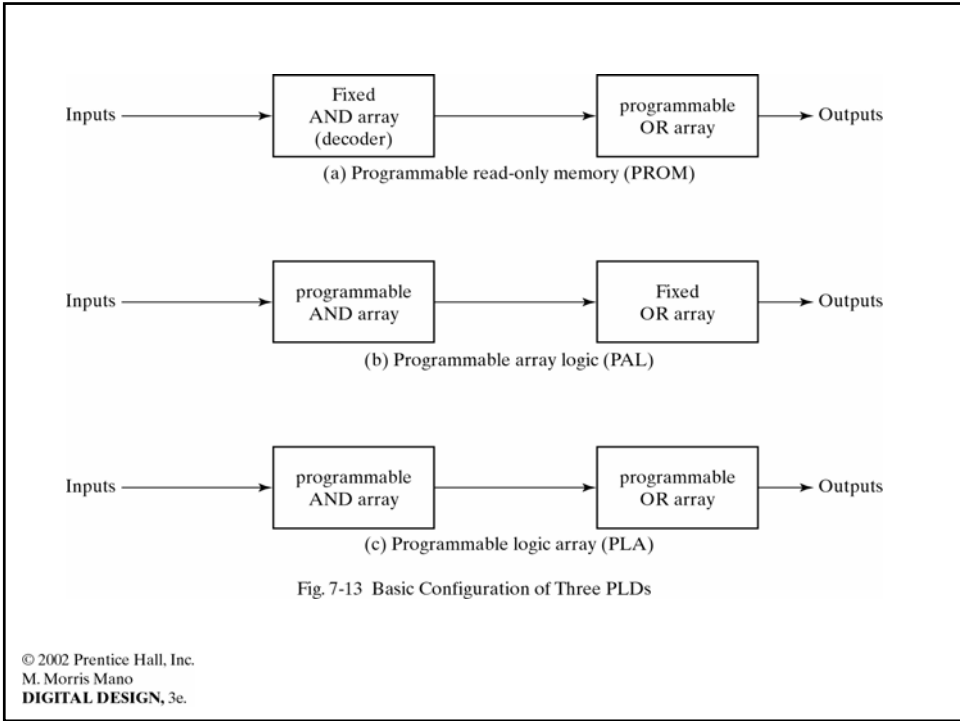
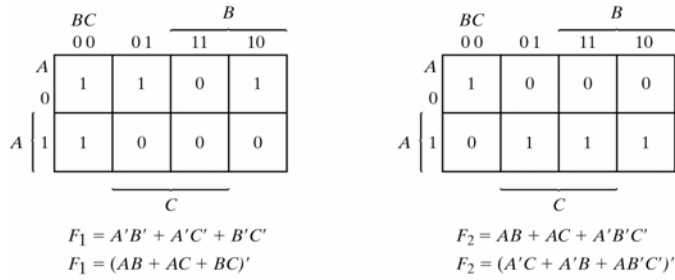


Fig. 7-10 Internal Logic of a  $32 \times 8$  ROM

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PLA programming table

Product term	Outputs					
	Inputs			(C) (T)		
	A	B	C	F <sub>1</sub>	F <sub>2</sub>	
AB	1	1	1	-	1	1
AC	2	1	-	1	1	1
BC	3	-	1	1	1	-
A'B'C'	4	0	0	0	-	1

Fig. 7-15 Solution to Example 7-2

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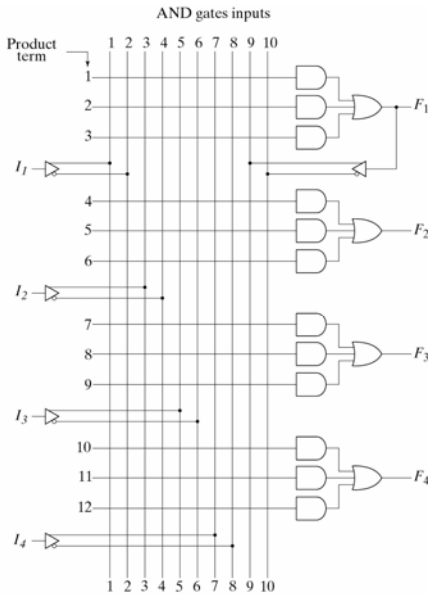
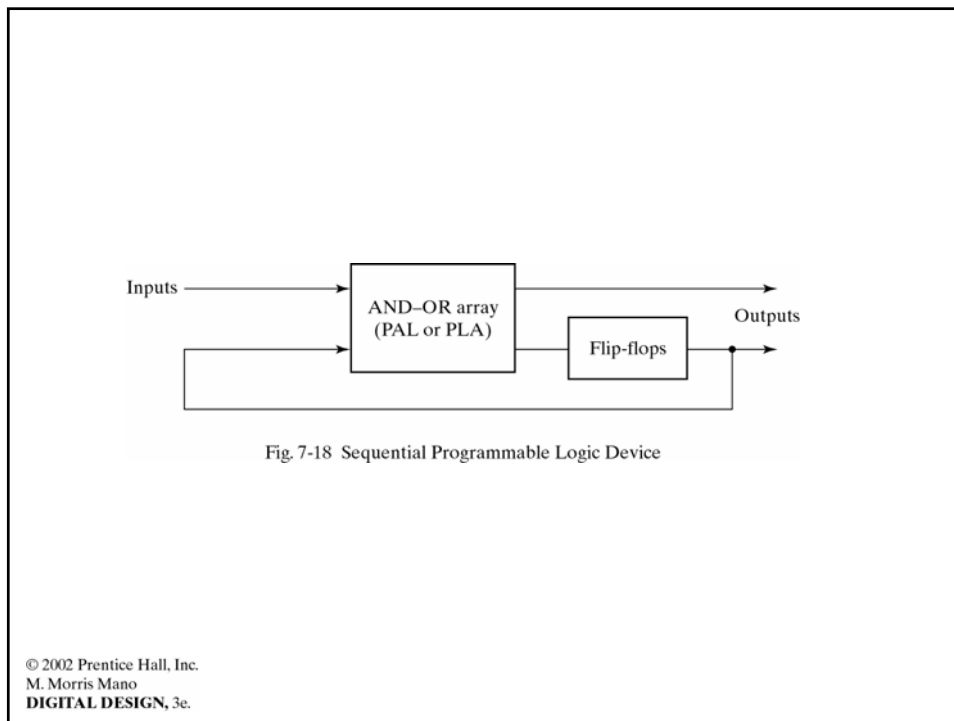
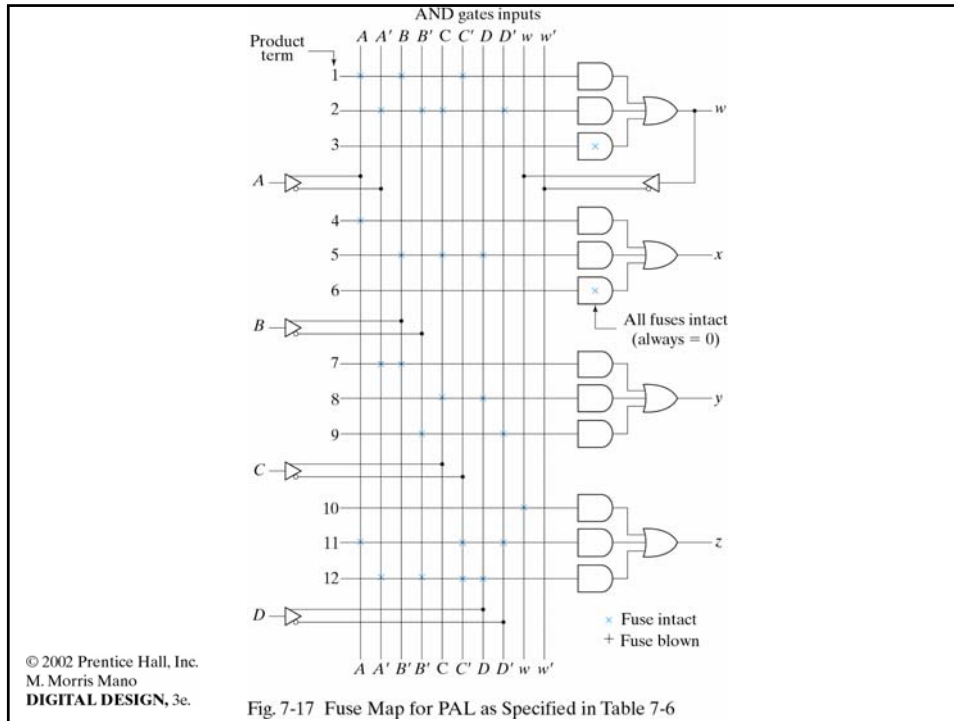
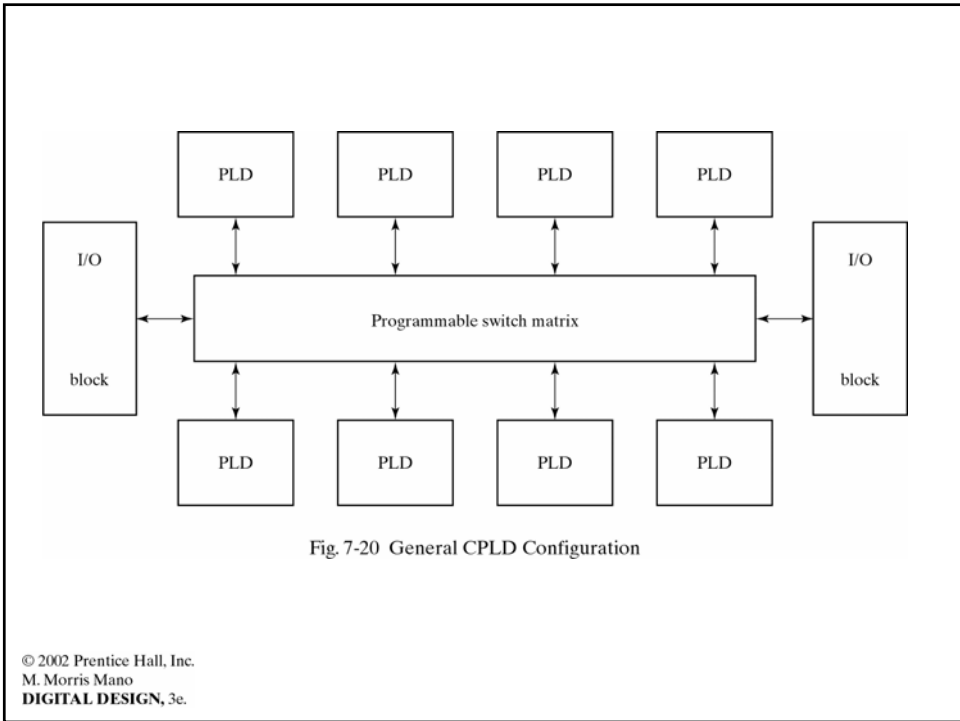
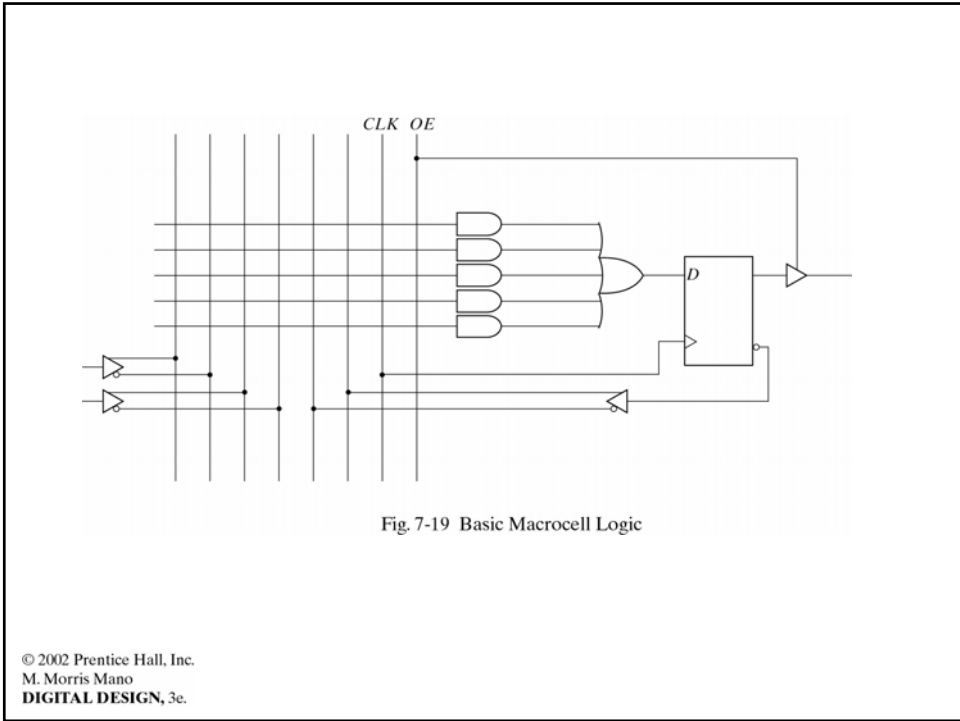


Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

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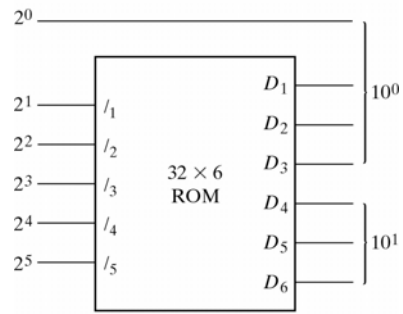


Fig. P7-17

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