Thermal Runaway Avoidance during Burn-in

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ABSTRACT

In deep sub-micron technologies, increased standby leakage current in high performance processors results in increased junction temperature. Elevated junction temperature causes further increase on the standby leakage current. The standby leakage current is expected to increase even more under the burn-in environment leading to still higher junction temperature and possibly the thermal runaway. In this paper we investigate the thermal management of high performance processors during burn-in.

1. Introduction

Stressing during the Burn-in (BI) accelerate the defect mechanisms responsible for early life failures. Thermal and voltage stresses increase the junction temperature resulting in accelerated aging. Elevated junction temperature, in turn, causes leakages to further increase by approximately 3-4x, going from nominal to burn-in conditions. In nano-meter regime, this may result into positive feedback leading to the thermal runaway. Figure 1 shows a chip that has gone to thermal runaway. To avoid thermal runaway, it is crucial to understand and predict the junction temperature under the normal and stress conditions. Junction temperature, in turn, is a function of ambient temperature (T_a), junction to ambient thermal resistance (R_{ja}), and static power dissipation.

2. Junction Temperature Estimation Procedure

The junction temperature (T_j) of an IC is defined as the average temperature of the silicon substrate. The junction temperature or T_j , is defined as [2]:

$$T_j = T_a + P \times R_{ja} \quad (1)$$

where T_a is the ambient or set point temperature, P is the device total power, and R_{ja} (R_{th}) is the junction-to-ambient thermal resistance. The power dissipation can be subdivided into dynamic and leakage components, as:

$$P = P_{Dynamic} + P_{Leakage} \quad (2)$$

$$P_{Leakage} = V_{DD} \times I_{Leakage} \quad (3)$$

$$P_{Dynamic} = C \times V_{DD}^2 \times f_{toggle} \quad (4)$$

In equation 4, C is the total IC switching capacitance and f_{toggle} is the frequency that is used for node toggling during burn-in and is expressed as:

$$f_{toggle} = \frac{I_{on}}{C_{gate} \times V_{DD} \times N} \quad (5)$$

where C_{gate} is the gate capacitance of a single gate and N is the number of logic stages in the critical path. To evaluate junction temperature, T_j , under different environmental conditions, a program and a methodology has been developed (Fig 2) [3,4].

3. Simulation Results

A 32-bit microprocessor in 130 nm dual V_T CMOS technology was used to verify the procedure. The parameters of this program were calibrated to the experimental data from the microprocessor. As illustrated in the Figure 3, for air-cooled BI ovens if the T_a is kept above 10°C, the T_j starts rising and does not

converge. This rise in temperature will lead the chip to thermal runaway. The same chip in liquid cooled BI oven (solid lines) will tolerate up to 76°C of T_a , which results in 110°C of T_j . Liquid cooled BI ovens with R_{ja} of 0.5°C/W are able to transfer more heat from the chip than air cooled BI ovens R_{ja} of 1.5°C/W. Since the total power at BI condition ($T_j=110^\circ\text{C}$, $V_{DD}=1.8\text{ V}$) for this chip is 66W, 1°C/W reduction in R_{ja} will allow us to perform BI in 66°C higher T_a . The results in Figure 3 confirm that the T_a is increased from 10°C to 76°C in liquid cooled BI ovens. It should be noted that since the ambient temperature in air-cooled ovens cannot be less than the room temperature, it is impractical to burn-in this microprocessor in air-cooled BI oven as at room temperature ambient, the chip will eventually go to thermal runaway.

Simulations were carried with 10% reduction in channel length of the transistors in 130 nm technology to incorporate process variations. This resulted in ~3x increase in the sub-threshold current and consequently ~3x increase in leakage power. Figure 4 illustrates the simulation results of the chip with 10% smaller channel length transistors than nominal value in 130 nm technology. As it can be seen in the Figure 4, the ambient temperature must be reduced from 76°C to 30°C for liquid cooled BI oven to maintain T_j at 110°C. Since it is difficult to maintain the T_a in BI ovens around room temperature, it is necessary to reduce the R_{ja} of the BI oven. The next generation BI ovens are expected to have R_{ja} of 0.3°C/W using refrigeration as a cooling solution and R_{ja} of 0.25°C/W using spray cooling technique as cooling solution, respectively. With R_{ja} of 0.25°C/W, this processor can be burnt-in in the ambient temperature of 70°C.

4. Thermal Runaway

As mentioned before, temperature and leakage current are strongly correlated and create a positive feedback mechanism. Under BI or normal operating conditions, designers try to control the T_j by removing the heat from the chip. As long as the rate of heat removal is greater or equal to the rate of heat generation, the T_j remains constant at the designed operating point. When the rate of heat generation becomes greater than the rate of heat removal, T_j starts to increase and thermal runaway occurs. Figure 5 shows the transient behavior of R_{ja} . When the chip is powered on, the R_{ja} starts to increase and reaches to its steady state condition, which as a typical example is 0.6°C/W.

In Figure 6, straight lines are drawn using Equation 1, which can be expressed as:

$$P_{removed} = (T_j - T_a) / R_{th}$$

with ambient temperature of 35°C. As time increases, the thermal resistance increases from 0°C/W and reaches to steady state value of 0.6°C/W. Hence, the straight lines represent transient behavior caused by changing thermal resistance with time. On the other hand, the exponential curve is the generated leakage power or chip leakage power at a given T_a . The intersection of the straight line (representing the removed power) and the exponential curve (representing the leakage power) represents the steady state operating condition of the system where removed heat is equal to the generated heat. As long as there is an intersection between removed power curve and chip power curve, thermal runaway will not occur.

In Figure 7, the leakage power of the chip with nominal leakage and the leakage power of the chip with high leakage due to 10% shorter channel length, versus the T_j are depicted. It can be seen that the leakage power for the nominal leakage chip has an intersection with removed power curve at 110°C. The slope of the line is 1/0.5°C/W and the T_a is 80°C. At higher temperature than 110°C the removed power is larger than the chip leakage power and in lower temperature than 110°C the leakage power is higher than removed power. This means that from any point in the neighborhood of 110°C the temperature will return to 110°C, which is the design point for BI condition. On the other hand if we look at the curve for the high leakage chip, we see that there is no intersection between this curve and the removed power curve with R_{ja} of 0.5°C/W. Since at all temperatures the removed power is less than leakage power, for this particular chip, the BI environment will lead the chip to thermal runaway. To overcome the problem the BI environment must be changed. The new environment is shown in the figure with R_{ja} of 0.25°C/W and T_a of 70°C. From this experiment, it can be concluded that for scaled chips with higher leakage power, the setup for BI environment must evolve by either reducing one of the T_a and R_{ja} or a combination of both of them. This will shift the removed power curve to the left to intersect the leakage curve of generated power for IC at the designed BI condition.

5. Conclusion

In this paper, we investigated the thermal management of high performance chips in the BI environment. An electro thermal analysis tool was developed to analyze thermal runaway possibilities due to self-heating under burn-in environment. It was

Fig 1. Test socket destroyed by thermal runaway [1].

Fig 2. A Procedure for junction temperature estimation [6].

Fig 3. Steady state T_j for 130 nm high performance microprocessor at BI condition.

Fig 4. Steady state junction temperature under Burn-in conditions for a 130 nm Microprocessor with 10% smaller channel length.

concluded that in order to avoid the thermal runaway, the burn-in environment must be set up such that the chip power at any temperature higher than BI temperature be less than removed power so the junction temperature converges to the BI design point temperature.

References:

- [1] Mark Miller (AMD), "Next generation burn-in & test systems for Athlon microprocessors: hybrid burn-in," Burn-in and Test Socket Workshop, Session 5, 2001.
- [2] P. Tadayon, "Thermal challenges during microprocessor testing," *Intel Technology Journal*, Q3, pp. 1-8, 2000.
- [3] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design Impact of Positive Temperature dependence on Drain Current in Sub-1-V CMOS VLSIs," *IEEE Journal of Solid-State Circuits*, VOL. 36, NO. 10, Oct. 2001.
- [4] A. Vassighi, O. Semenov, M. Sachdev, and A. Keshavarzi, "Thermal management of high performance microprocessors in burn-in environment," *Proc of 18th IEEE International Symposium on Defect and Fault tolerance in VLSI Systems*, 2003.

Fig 5. Thermal resistance increases with time and reaches to its steady state value of 0.6°C/W.

Fig 6. 130 nm microprocessor leakage power (exponential) and removed power (straight lines) for thermal resistance of 0.6°C/W.

Fig 7. Burn-in setup points for nominal leakage and high leakage chips.